EDWARD H.W. LIU

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SUMMARY

Engineering student specializing in embedded systems, real-time operating systems (RTOS), and hardware-software integration. Proficient in C++, Python, and Verilog, with practical experience in FPGA programming, signal processing, and system optimization. Hands-on expertise with computer vision, digital logic design, and algorithm development, including applications of OpenCV, multithreading, and hardware debugging tools. Demonstrated ability to work with memory management, schematics, and digital interfaces to achieve efficient system performance.

EDUCATION

University of Toronto **Sept. 2022 – Apr. 2027 (expected)**

Bachelor of Engineering (BASc) in Computer Engineering + PEY Co-op, Minor in AI, and Business

Cumulative GPA: 3.90/4, Dean's Honour's list

Relevant Courses: *Operating Systems/Computer Fundamentals/Computer Organization (C/Assembly), Programming Fundamentals/Communications & Design (**C++**), Applied Fundamentals of Deep Learning (**Python/Pytorch**/Keras)*

SKILLS

Technical Skills:

- Coding Languages: C++, Python, Java, C#, Javascript
- Library/Frameworks: Pytorch, Tensorflow, numpy, pandas, React.js, OpenCV, Albumentations, Spring boot

Professional Skills:

- Project management/Teamwork
- Organization and Prioritization
- Attention to detail

PROFESSIONAL EXPERIENCE

Software Engineer **Jun 2025-Aug 2026**

Qualcomm | Markham, Canada

- Built a fully automated Jenkins CI/CD pipeline from scratch, streamlining integration across repositories and reducing pipeline time by 800%
- Developed and optimized video driver functionality integrated with advanced VPU architectures for next-generation automotive and multimedia systems
- Profiled performance across interdependent components, improving end-to-end processing throughput by 20%

TECHNICAL ENGAGEMENTS/PROJECTS

Journey of the Prairie King Recreation **Oct - Dec 2023**

- Developed **RTL** for an **FPGA**-based game using Verilog, showcasing digital logic design and hardware interfacing. Focused on efficient data handling and timing constraints to ensure smooth gameplay
- Designed and implemented game logic on an ARM-based DE1-SoC **FPGA** using **Verilog**, optimizing digital circuit design for efficient data handling through **VGA** and **PS2** interfaces, resulting in a 95% bug-free hardware interaction
- Managed memory allocation and timing using on-board **SDRAM**, ensuring efficient data retrieval and storage for real-time game operations, while debugging signal paths with Quartus and logism, resulting in improved system performance

Angry Birds Recreation **Apr - May 2024**

- Developed physics and game mechanics using **C** on a **DE1-SoC FPGA**, creating shooting dynamics, collision detection, and player interactions, ensuring smooth and accurate gameplay through **efficient resource management** on the FPGA.
- Implemented **double-buffering** in C for smooth rendering of game frames, reducing screen tearing and improving visual performance during high-speed game sequences.
- Integrated **PS2** keyboard controls and **audio** output, synchronizing real-time player input with background music and sound effects using FPGA audio controllers, **optimizing hardware interaction** for an immersive and responsive user experience.

Data and Systems Engineer, Advanced License Plate Recognition Project **May - Aug 2024**

- Developed a real-time license plate recognition system using **YOLOv10, custom EasyOCR** and **PyTorch**, achieving **95%** accuracy in character recognition through optimization and fine-tuning of deep learning models
- Preprocessed and augmented data with **python albumentations** and **openCV** library, significantly improving model performance and robustness
- Integrated VGG feature extractor, **CNN**s, and **attention** mechanisms in **Python**, optimizing inference times for distributed systems by 20%.

Team Leader, Evie Mapping Application **Jan - Apr 2024**

- Developed a **C++** and **Glade** Open Street Map Application for Electric Vehicle owners, integrating global charging station data and stop planning functionality, enhancing route optimization and usability compared to existing solutions
- Implemented and optimized **Dijkstra's, A, Ant Colony**, and **Simulated Annealing** algorithms for efficient pathfinding and **resource optimization**, enabling optimal route planning that was 15% faster for long distances
- Utilized **multithreading** and efficient datastructures to achieve a 20x reduction in computation time